The Office of Technology Management

UNIVERSITY OF TEXAS 🗡 ARLINGTON

Tech ID: UTA 16-31

Technique for Fabricating Ferroelectric materials on Semiconductors

INVENTORS: Joseph Ngai, Kamyar Ahmadi-Majlan, Mohammadreza Jahangir-Moghadam

TECHNOLOGY NEED

Ferroelectrics integrated on semiconductors have long been proposed to serve as a materials platform for a variety of technologies ranging from sensing to computing. In regards to computing, ferroelectrics on semiconductors could lead to field-effect transistors that require very little power to operate, or that integrate both logic and memory functionalities together. The development of such device technologies has become increasingly imperative as present semiconductor devices have reached fundamental limits in performance. Prior attempts to integrate ferroelectrics on semiconductors to realize field-effect transistors have been hampered by poor interfaces between the ferroelectric and semiconductor, and poor ferroelectric behavior at the nanoscale film thicknesses required for applications in computing.

INVENTION DESCRIPTION/SOLUTION

Researchers at UT Arlington have discovered a new ferroelectric material (SrZr_xTi₁-xO₃) that can be integrated on semiconductors with excellent interfaces. More remarkably, this ferroelectric material exhibits exceptionally robust ferroelectric behavior at nanoscale film thicknesses. The realization of a materials platform combining nanoscale ferroelectrics and semiconductors opens the pathway to realize a host of computing device technologies that possess both logic and memory functionalities, require little power to operate, and that are amenable to current paradigms in device size scaling.

APPLICATIONS

- Semiconductor devices
 - Field-effect transistors
 - Metal-oxide semiconductor capacitor
 - > Temperature and pressure sensors

KEY BENEFITS



More about the Inventors: Joseph Ngai

Contact information For licensing, please contact Koffi Selom Egbeto (Licensing Associate) koffi.egbeto@uta.edu otm@uta.edu P: 817.272.1132

Our mailing Address: The Office of Technology Management 701 S Nedderman drive, Suite 350, Arlington, TX 76019

- Improved performance
- Reduced power consumption
- Increased functionality e.g. combines both logic and memory functionalities

STAGE OF DEVELOPMENT

Extensive tests

INTELLECTUAL PROPERTY STATUS Patent pending



Connect with us: in 🈏